Communications
Research
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S-BAND ADAPTIVE RADAR SYSTEM

by

A.L. Poirier

This work was sponsored by the Department of National Defence,
Research and Development Branch under Project No. 041LC13.

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COMMUNICATIONS RESEARCH CENTRE

DEPARTMENT OF COMMUNICATIONS
CANADA

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(Radar and Communications Technology Branch)

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Abstract

An experimental S-band phased-array radar system developed at the Communications Research Centre is described. The system was developed to provide experimenters with a means of acquiring real-time radar data for on-line or off-line analysis and to establish a test bed for new experimental devices or data processing techniques.

The system is built in modular form, thus allowing various parts of the system to be easily interchanged with experimental devices. It is linked to a Digital Equipment Corporation 11/780 VAX computer which allows data to be transfered from the radar to the VAX in real time, or to be stored in high-speed buffers and then transferred in blocks directly from the buffers to the VAX. The experimenter, using the VAX, can adaptively control the radar, request new beam directions, control data acquisition, etc., via the link.

1. Introduction

The Adaptive Radar facility at the Communications Research Centre, Radar Research Laboratory, is based on an experimental phased-array antenna on long-term loan from the Royal Signals and Radar Establishment in the UK. It was developed as a research tool to study advanced techniques applicable to military radars. In addition to the research required during development, the facility provides a means by which experiments may be undertaken on a variety of radar signal and data processing techniques. Up to the current state of development, the system has been constructed and maintained and experiments undertaken by a combination of CRC and contracted support staff. However, much of the design and the management of the project have been provided by the CRC in-house staff.

2. Background

The development of the radar has been part of an in-house project that started in 1975 as a long-term research study into advanced techniques applicable to military radars. The motivation for this research study stemmed from the realization that, for many applications, the air surveillance and tracking requirements of Department of National Defence (DND) could best be met in the future by radars using electronically-scanned antennas and extensive digital processing. No experience with such radars existed in Canada and it was considered essential to correct this deficiency so that Department of National Defence (DND) could appreciate the potential of these advances, as well as their problems. DND would thereby be in a position to specify its future requirements in full knowledge of the state-of-the-art, and to evaluate the new radar systems being considered for procurement. At the same time, the basis would be laid for possible development in Canada of radar systems or subsystems, whether in collaboration with other countries or solely

nationally, taking advantage of Canada's industrial strengths in digital processing technology.

As the system has evolved, experiments have been conducted which have demonstrated enhanced capabilities of the system by the use of novel digital processing techniques originated within the project.

3. General Description

The system consists of a 295-element space-fed lens array (Figure 1) a computer-controlled transmitter and receiver, various time control subsystems, signal processors, and analysis facilities, (Figure 2). The radar is controlled by three computers; one to control the phased-array antenna and the radar system with its various sub-systems; a second to perform such functions as plot extraction and control of displays, and the third to act as a tracking computer and for the use of experimenters to provide in-depth analysis of return data.

The array antenna is designed to cover a sector of ±40 degrees in azimuth and ±30 degrees in elevation. As the plane of the array is vertical, its boresight is horizontal and the elevation look angles must be restricted to the range 0 to +30 degrees. The antenna is set on a rotatable turntable, (Figure 3), and can be positioned to face any of three radar windows separated in angle by 60 degrees. This allows a total coverage of 200 degrees in azimuth. However, rotating the turntable is not an adaptive feature of the system and the turntable is usually fixed in position for any given experiment.

The phased-array antenna, transmitter and receiver front-end are housed in a small radar laboratory mounted on the roof of the main radar building penthouse. The computers and remainder of the radar system are located in the main building.

The radar is controlled from a control computer terminal. An operator-interactive program in the control computer allows the operator to enter the required radar parameters, scanning and other operating instructions through the terminal keyboard and to monitor the radar's responses through the terminal display.

Built-in fault-finding detectors are included in both the hardware circuits and the control software so that malfunctions can be detected and their cause quickly located. The system is automatically protected against possible damage when breakdowns occur in critical parts of the system or when wrong instructions from the operator could cause possible damage, such as too high a duty cycle in the transmitted radar pulses. The detection of such faults inhibits the turn-on of the system and sends back a warning message to the operator. The name of the affected subsystem and the type of fault detected are displayed on the terminal.

Radar return data can be collected in real-time and stored on disk or magnetic tape for later analysis. This is done by means of high-speed

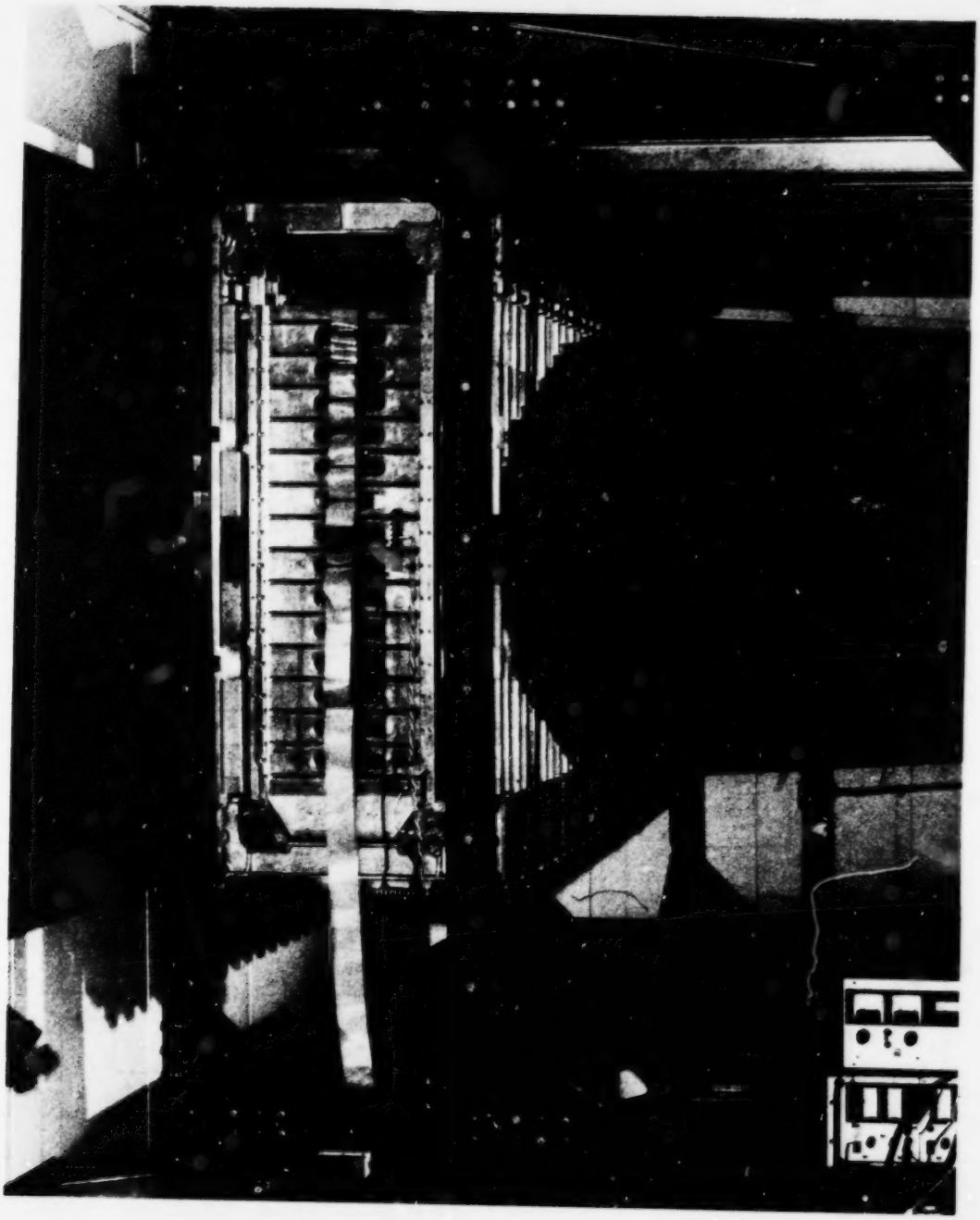


Figure 1 - Space-Fed Lens Array

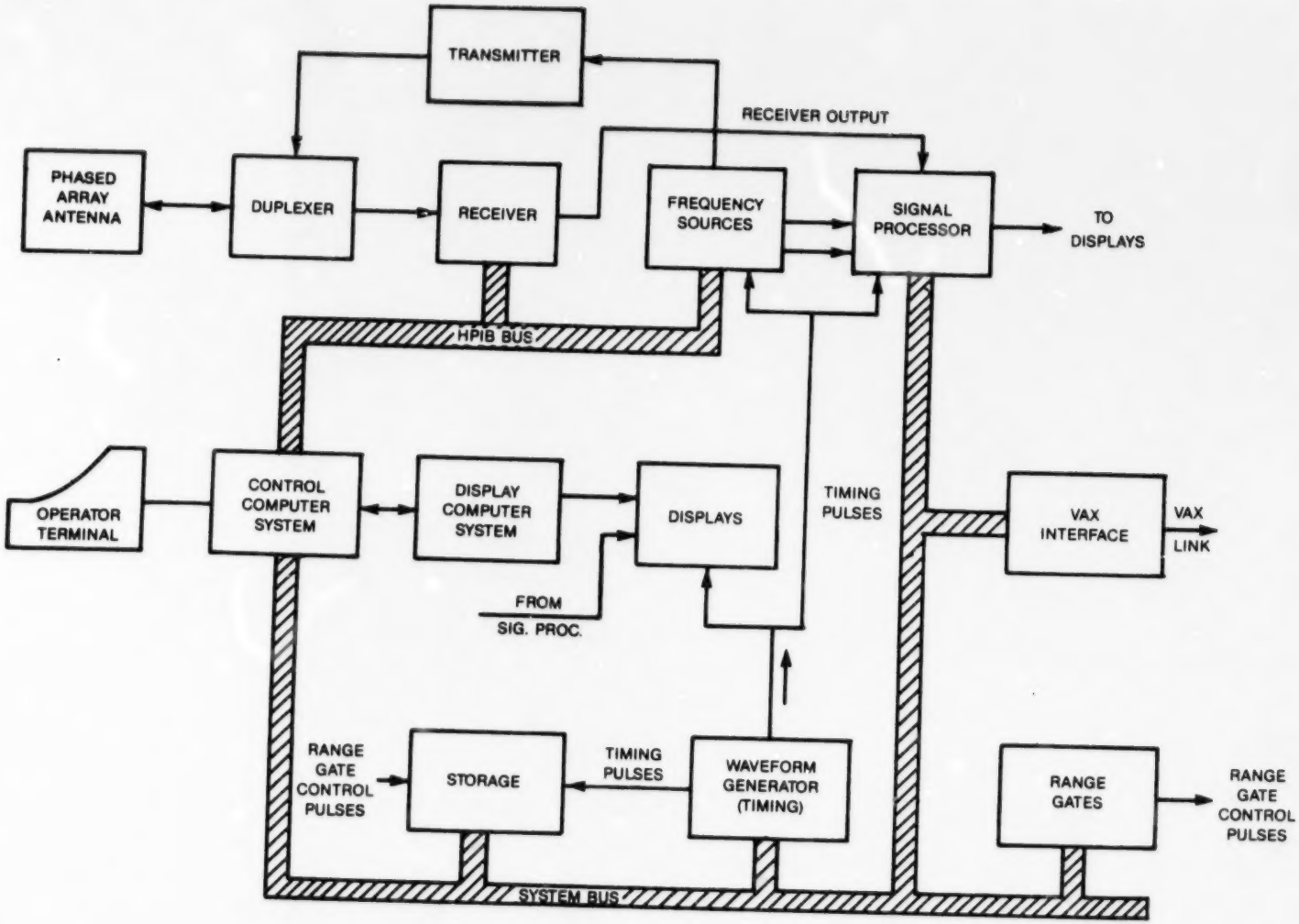


Figure 2 - Basic System Diagram

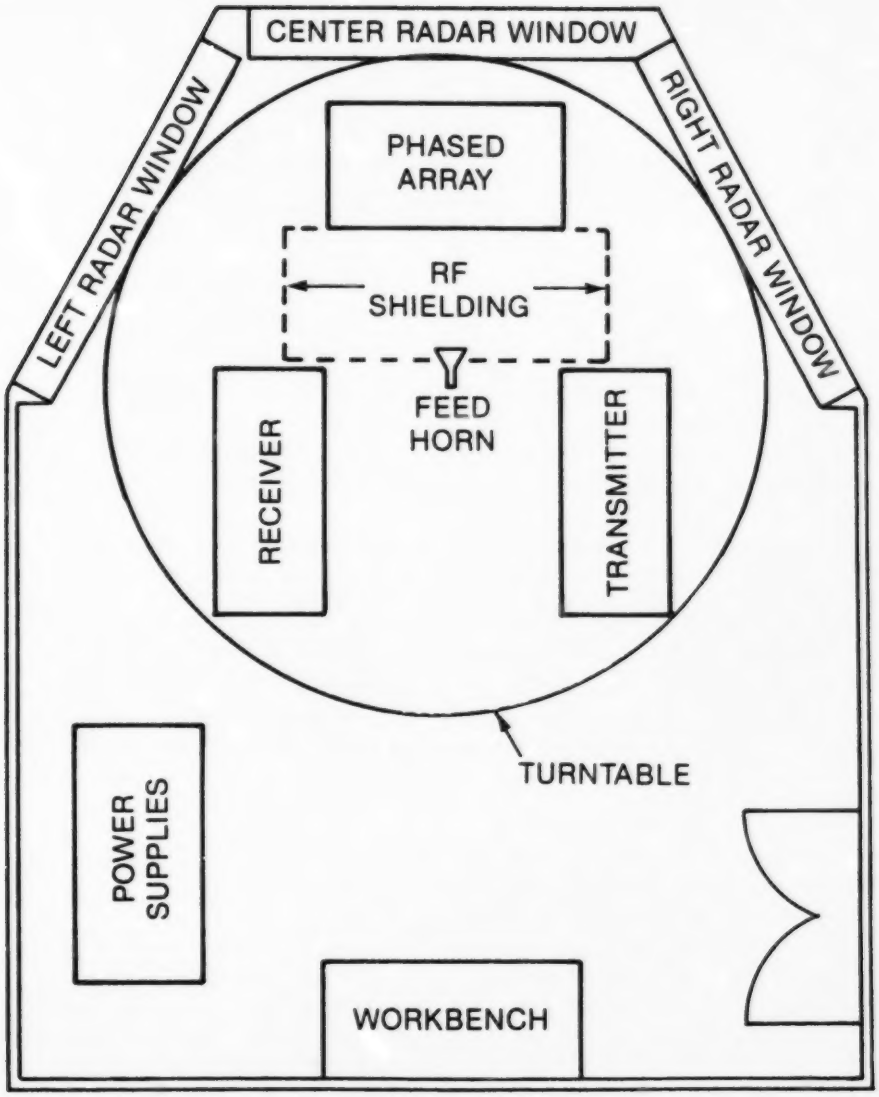


Figure 3 - Penthouse Radar Laboratory

buffers in which blocks of data can be entered in real-time and transferred to disk or tape at a slower rate. The data can also be transferred via a link to a Digital Equipment VAX 11/780 computer for analysis or target tracking purposes, or for storage in the VAX storage facilties for later analysis.

4. Detailed Description

4.1 Phased Array Antenna

The antenna array consists of 295 elements arranged in an elliptical pattern 1.1 metres in height by 1.6 metres in width (Figure 4). Each element consists of 2 in-line horns, 3 RF phase shifters (Figure 5a), and control circuits. The elements are arranged into 27 columns containing a minimum of 2 elements in the end columns and a maximum of 15 in the centre columns. A daisy-chain flat ribbon bus couples each element in each of the columns to a central array driver which in turn couples the array back to the control computer. Each element is assigned an address related to its physical position in the array (Figure 4) and can be addressed individually by the control computer. Some instructions are global and can address all the elements simultaneously. This allows single instructions to perform such functions as resetting or steering the array.

The array is essentially a lens which focusses an RF signal from a feed horn, located approximately 1 metre behind the array, into a steerable beam. This is accomplished by setting the phases through each of the array elements so that the total resultant signal emanating from the front of the array has a uniform phase-front in the direction in which the beam is steered. The feed horn is designed so that the illumination on the array backplane is a maximum in the centre of the array and 10 dB down around its outer periphery. Conversely, as the array is reciprocal, signals received from the direction in which the beam is steered are focussed into the feed horn.

Each element is driven by a controller mounted directly on the element. The main functions of the controllers are to steer the array and monitor its performance. Phase settings can be applied to the array either on an element by element basis or globally by reading prestored settings from 4K RAM memories on each of the element controllers. The controllers continuously monitor the performance of the elements and send fault warnings back to the computer when malfunctions are detected. The controller can write to and read from the element memories, perform various tests on the elements, and otherwise perform all the functions necessary to control the array.

The RF portion of each element consists of the two in-line horns pointing in opposite directions and coupled together through controllable phase-shifters (Figure 5(a)). The phases through the phase-shifters can be selected in 45-degree increments from 0 to 360 degrees. Because of the large number of elements in the array and the effects of averaging, the use of 45-degree increments allows the beam to be stepped in azimuth and

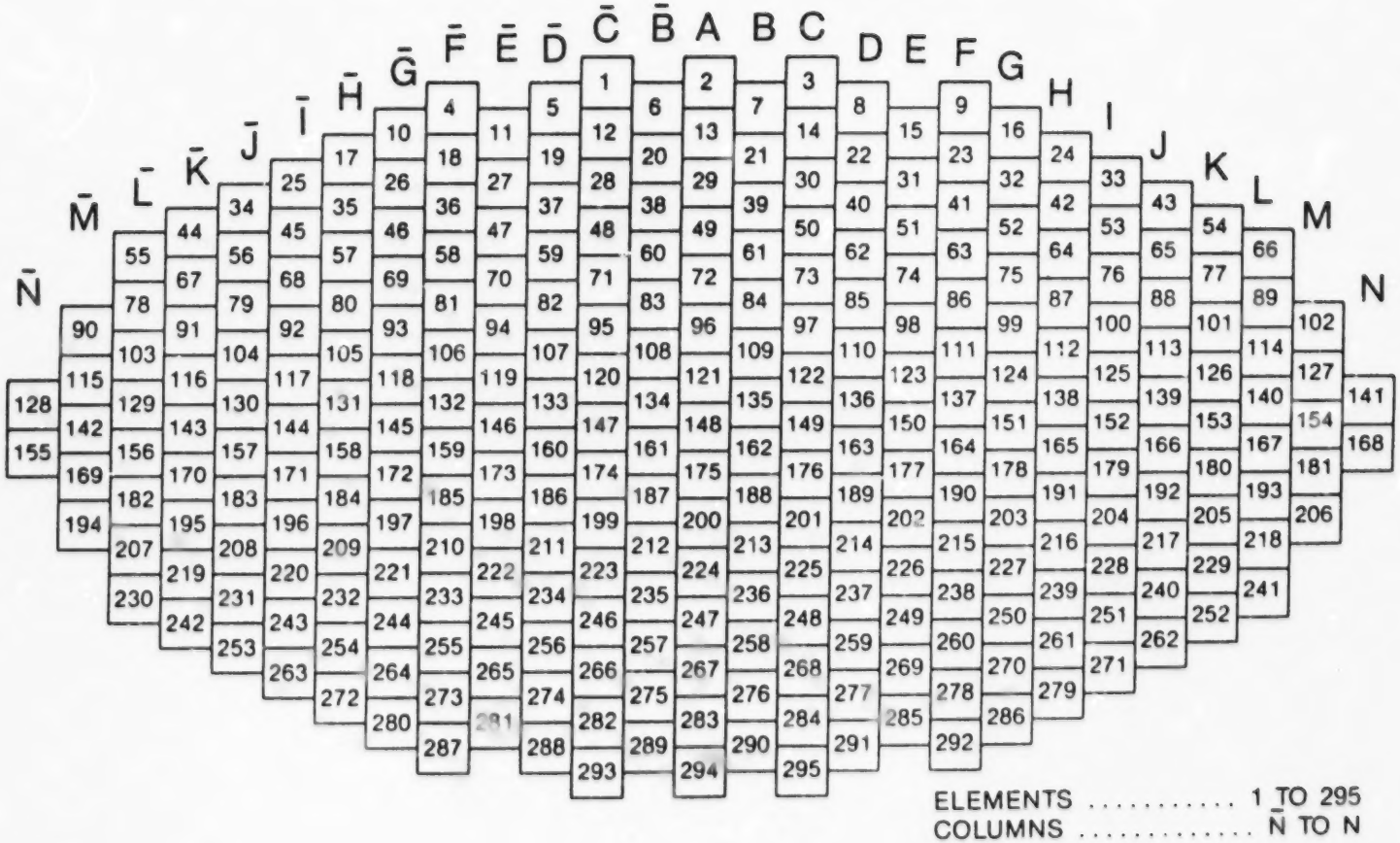
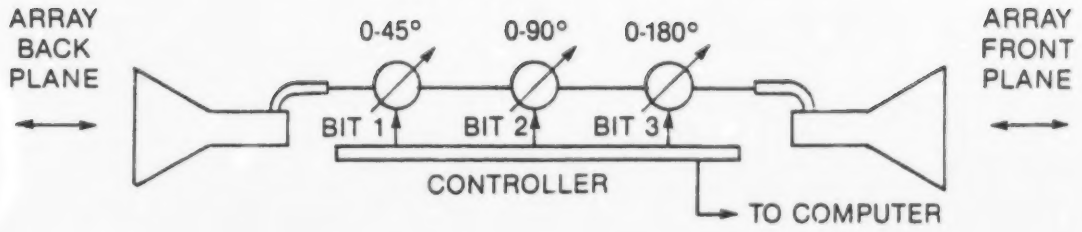
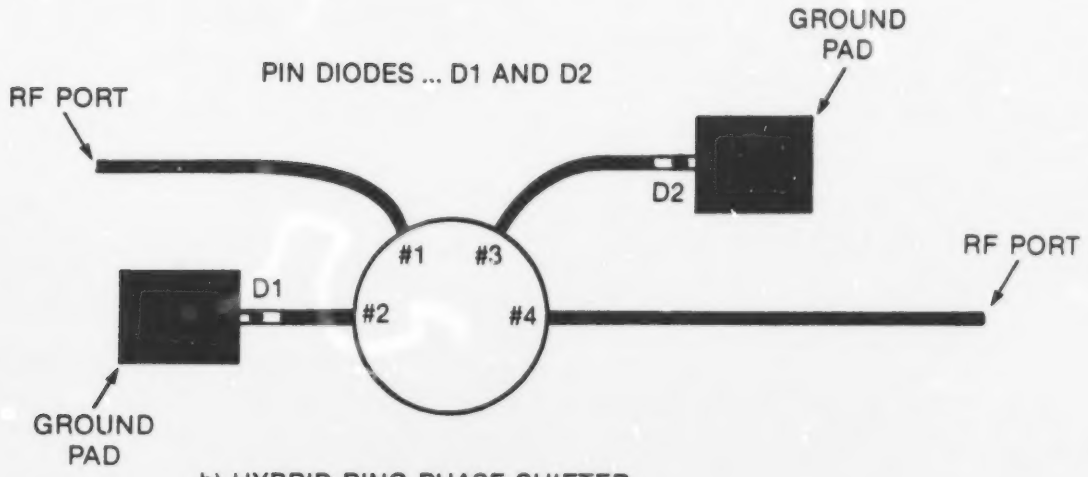


Figure 4 - Array Numbering System - Rear View



a) ELEMENT PHASE-SHIFTER CONFIGURATION



b) HYBRID RING PHASE SHIFTER

Figure 5 - Phase Shifters

elevation in increments of less than 0.1 degrees. Note: In practice, the step increments are limited to 1.0 degree in order to restrict the total number of look directions to the 4K capacity of the element RAMs.

The phase-shifters consist of three hybrid rings and six phase-shifting pin diodes (3 pairs). The first phase-shifter switches between 0 and 45 degrees, the second between 0 and 90 degrees, and the third between 0 and 180 degrees. The hybrid rings are arranged so that a signal entering port #1 divides between ports #2 and #3 (Figure 5(b)). These ports connect to lines terminated in short circuits that reflect the signals back into the hybrid ring and phased so that the reflected signals cancel at port #1 and add at port #4. The pin diodes are located between the shorted terminations and ports #2 and #3, and change the effective positions of the shorts when they are conducting. The reflected signals passing through port #4 can thus be shifted in phase by the required amount, i.e., 45, 90 or 180 degrees.

The digital phase settings consist of 3-bit digital words. Each bit is fed to one of three analog drivers which control the diodes. When a bit is in the high state, the diode pair driven by that bit is switched ON. When the bit is in the low state, the diode pair is switched OFF. In this manner, digital settings fed from the computer can switch the diodes ON and OFF in the required manner. The phase settings can be sent directly to individual elements to steer the array or for entry in the RAM memory contained in each of the elements. Each RAM memory has the capacity to store 4096 3-bit phase settings accompanied by a parity bit for each setting. After the memories in the array have been loaded, the beam can be steered by reading the required settings from memory by a global 'READ' (beam-steering) command.

4.1.1 Fault Detection

Parity bits are used by the fault checking circuits in each of the element controllers. When a steering instruction with a wrong parity bit is sent to an element, the fault checking circuits set a bit in the status register and lower the array fault return flag. This causes a computer interrupt which in turn calls error checking routines in the main program.

In addition to parity checks, the controller continuously compares the bit settings applied to the diode drivers with those sensed across the diodes. The parity of the sensed setting is compared with the parity of the applied setting and, if a mismatch occurs, error bits are set in the element status register and the fault flag is lowered. The fault checking routines can then address each element individually until the fault is found. The actual settings across the diodes in any of the elements can also be read. This is used as part of the test procedure in which diode settings are sent to an element and read back. Faulty operation of the diode drivers or diodes can thus be detected.

Each type of error that can be detected is assigned a bit on the

array status register. The bits are set automatically when a fault occurs. The status register bit format is as follows:

```
Bit 0 .... 45-degree diode setting (sensed across the diodes)
    1 .... 90-degree    "     "        "       "    "    "
    2 .... 180-degree   "     "        "       "    "    "
    3 .... SKS1 error - wrong parity in instruction word
    4 .... SKS2   "   - wrong parity applied across diode
    5 .... SKS3   "   - wrong setting on diodes
    6 .... FAULT FLAG
```

Once a fault has been detected, the operator can, if necessary, disable the fault checking circuits in the faulty element so that malfunctions in other elements can be detected.

The fault detectors do not test the operation of the RF circuits. These can be tested by means of a calibrated source located approximately 1.5 kilometers from the radar or by a calibrated RF pulse that can be injected at the front end of the receiver. The calibrated pulse is controled in magnitude, timing and pulse-width by the radar control computer.

4.1.2 Synchronization

The array is synchronized to the radar by means of beam-switching pulses received from the waveform generator. The array interface is programmed so that the beam steering instructions are sent to the array, but are not acted upon until the beam-switching pulses are received. A beam switching pulse is sent twenty-five microseconds prior to each radar transmission. This allows the array time to switch the beam (when a steering instruction is received) and stabilize itself before the transmission actually occurs. The next steering instruction can be sent to the array as soon as the array has been switched. The computer is notified that the array is ready for the next instruction by an interrupt request from the array interface.

4.2 Radar Transmitter/Receiver System

The radar pulsed transmitter consists of a transistor amplifier chain driving a TWT final amplifier. It is fed from frequency-stable IF and RF sources (4.2.2) and triggered by timing pulses from the radar waveform generator. The receiver system is made up of computer-controlled modules that can be configured by the operator through the system control program. Various signal sources, filters, attenuators, etc., can be switched in or out of the system. A list of the parameters or subsystems that can be selected is given in Appendix A, items 2,3, and 4.

4.2.1 TWT Power Amplifier

The transmitter final power amplifier currently in the system is a Litton L-5569-51 TWT. This tube has a phase-coherent peak power capabil-

ity of 3.5 kW. If it becomes necessary to raise the output power level, phase-coherent power amplifiers capable of handling the higher power level can be inserted into the system. The phased-array antenna was designed to handle powers of up to one megawatt.

4.2.2 Frequency Sources

The transmitter frequency is derived by mixing a gated local oscillator signal with a gated IF reference signal. The resultant RF pulse is filtered and amplified to the required level to drive the final amplifier. The local oscillator signal is applied to the receiver to convert return signals to the required IF frequency. The IF reference signal is used to phase-coherently detect the IF signals and derive in-phase (I-channel) and quadrature (Q-channel) video signal components.

The local oscillator and IF reference sources can be either crystal-controlled oscillators or synthesizers. The synthesizers provide the system with a frequency-agile capability in the range 2.961 GHz to 2.983 GHz. In the crystal-controlled configuration, the IF reference source is a 60-MHz crystal-controlled oscillator followed by a x4 frequency multiplier. Either the 60-MHz signal from the oscillator or the 240-MHz signal at the output of the multiplier can be selected. Note: At the present time the receiver IF frequency being used in the system is 60 MHz.

4.3 Waveform Generator

The waveform generator produces the timing signals required to operate the radar. It is clocked by 15 MHz, 10 MHz and 1 MHz clock pulses derived from the 60 MHz IF reference signal. The 10 MHz clock is the basic clock in the system and runs continuously while the radar is operating. The 15 MHz clock triggers the range-sample pulses. The 1 MHz clock is used in some of the device interfaces to time their operation.

The radar pulse repetition interval (PRI) timing pulse is the main synchronizing timer in the radar system. It is derived by a count-down counter clocked by the 10-MHz clock. It is used as a reference pulse for other timing pulses in the system. These are timed to precede or follow the PRI pulse by some fixed time determined by the various counters and comparators in their individual control circuits. The array beam-switching pulse, for instance, is derived from a comparator in the PRI pulse counter circuit. The range-sample pulses are derived from a mod-N counter clocked by the 15-MHz clock, which in turn is gated on by a zero-reference delay. The zero-reference delay is gated on by the PRI pulse timing circuit.

As the timing pulses are derived from either the 10 MHz or 15 MHz clocks, the timing intervals are in units of 1/10 of a microsecond or in units of 1/15 of a microsecond, the latter being equivalent to 10 radar-metres in range. The counts required for the above are contained in timing registers which are loaded during the turn-on procedure of the radar.

The waveform generators produces the following timing pulses:

1) PRI - periodic ... 83 to 6553.5 microseconds (prf 153 Hz to 12 KHz)
   PRI - staggered .. up to 14 staggers, same range of intervals as periodic

2) PW ..... 0.2 to 4.0 microseconds (duty-cycle limited)

3) Zero-ref. delay .. 0.3 microseconds to PRI (delays range sample pulses)

4) Dwell ..... 1 to 255 pulses or continuous (Dwell = 0)

The PRF hardware timing circuits can operate at PRIs of less than 83 microseconds. However, for practical reasons, a lower preset limit of 83 microseconds was built into the system. Further, the software limits the lower PRI to approximately 300 microseconds.

Error checking circuits monitor the contents of the timing registers and shut down the waveform generator if times exceeding the preset limits are encountered. This provides the system with some measure of protection, notably against transmitter overload.

4.4 Signal Processor

4.4.1 MTI Filters

The signal processor consists of an MTI processor, a rounder and scaler, a combiner, an accumulator, a CFAR threshold detector and, because of the experimental nature of the radar, two high-speed buffers in which radar return data can be stored in real time for later off-line analysis or storage, Figure 6.

The MTI processor contains two digital MTI filters, one for the I-channel and one for the Q-channel, in which digitised video signals from the receiver phase-detector are processed to suppress returns from stationary targets. The radar returns are processed by the filters in groups of N pulses, where N is the cancellation ratio of the filters. Each return is multiplied by a filter coefficient and the products summed over N pulses. The summed products from the two filters are then combined and fed to the integrator. The coefficients are such that the summed products over N pulses cancel for returns from stationary objects, i.e. the sum of N coefficients for a given filter characteristic must equal zero.

The coefficients are stored in a 512x12 PROM. The PROM currently contains the coefficients required for a 3-pulse cancellation ratio. However, the coefficients required for other cancellation ratios can easily be entered in the PROM as the need arises. A suitable expression for calculating the coefficients for various cancellations ratios is given below.

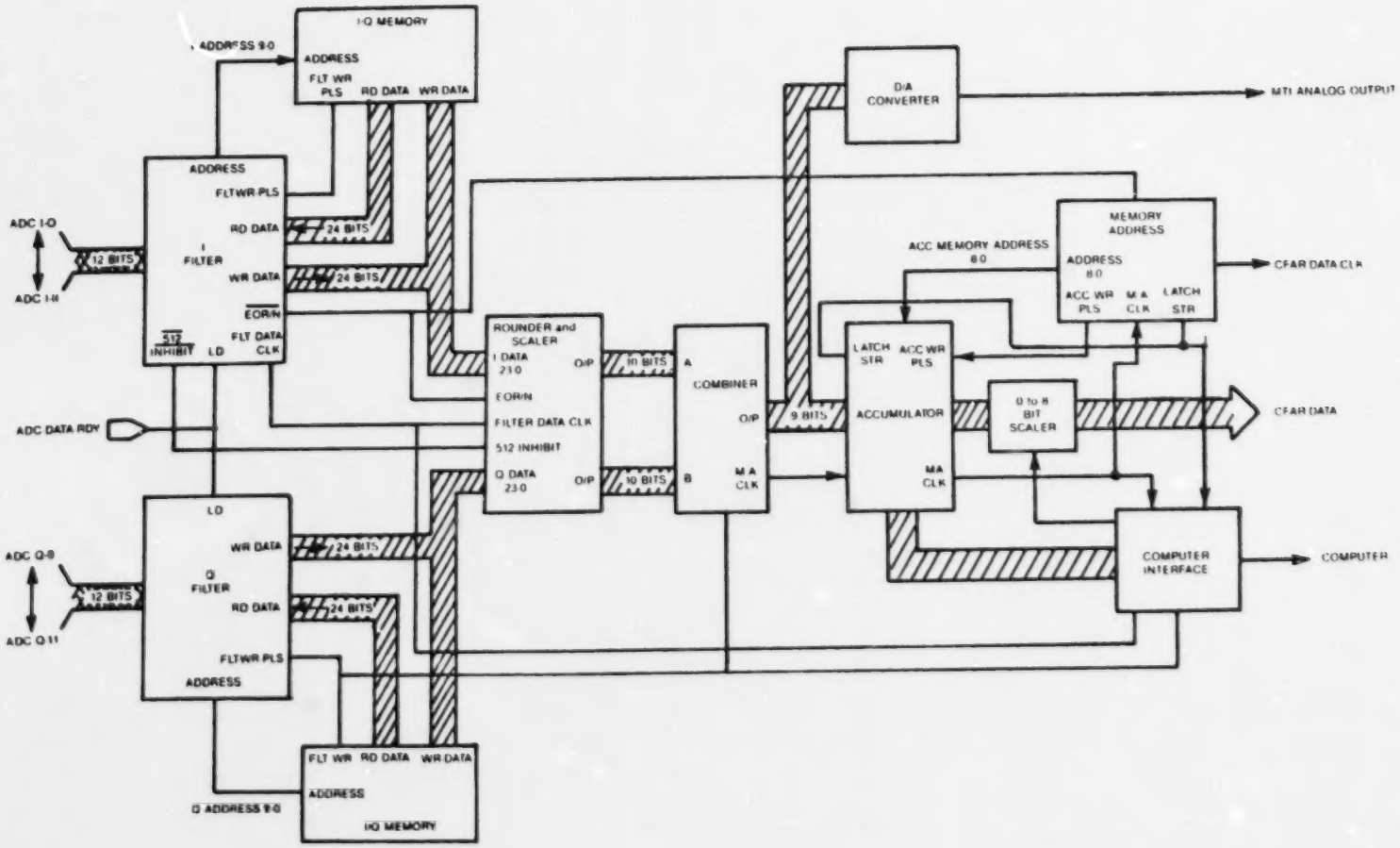


Figure 6 - Signal Processor

$$b_k = (-1)^k \binom{n}{k} \quad k = 0,1, \ldots, n$$

where

b_k = (Binomial) weight of k^{th} tap

n = Number of delay sections (moving window)

= Canceller order -1 (fixed window)

Using the above expression, the following sets are obtained:

2 Pulse Canceller (n=1) {1,-1}

3 Pulse Canceller (n=2) {1,-2,1}

4 Pulse Canceller (n=3) {1,-3,3,-1}

5 Pulse Canceller (n=4) {1,-4,6,-4,1}

6 Pulse Canceller (n=5) {1,-5,10,-10,5,1}

7 Pulse Canceller (n=6) {1,-6,15,-20,15,-6,1}

Each pulse within the group being processed by the filters (N pulses) requires a different coefficient. The coefficients are contained in an internal Programmable Read Only Memory (PROM) and can be read out and applied to the filters as required. The PROM can hold up to 512 12-bit coefficients. These are grouped into blocks, each containing the coefficients required for a given filter characteristic.

A pointer is initially loaded with the PROM address of the first coefficient of the selected block. After all returns from the pulse have been processed and fed to the filter memories, the pointer is incremented in preparation for returns from the next pulse. The pointer is incremented by the end-of-range pulse (beam switching) which occurs 25 microseconds prior to transmission of the next radar pulse. When returns from the last pulse in the group are being processed, the results from the two filters are combined and transferred to the integrator. During the transfer both filter memories are cleared. Upon completion of the transfer, the coefficient pointer, which is common to both filters, is reloaded to point to the first coefficient in the group. The filter can then process returns from the next block of pulses.

Returns from each range cell are processed separately. The memories in the MTI filters and the output integrator each contain 512 memory cells, so that returns from up to 512 contiguous range cells can be pro-

cessed. All returns in a given interpulse period are processed with the same coefficient. After a return is processed, it is stored in its own range slot in the MTI memories. Processing a group of pulses implies processing up to N x 512 individual samples in each filter for each pulse. The MTI filters have the ability to process one I- and one Q-channel return from each range cell, store the results in the MTI memories and be ready to process returns from the next range cell within the time interval between range sample pulses.

As implied above, a pass through the MTI filters consists of processing N pulses. The filters can operate in single-pass mode or in batches of M passes, where M can be specified by the operator. To avoid overflow, an upper limit is set for M which is determined by the magnitude of the signals and the word size of the integrator. Other factors of an operational nature also limit the size M, such as the maximum practical dwell time on target.

4.4.2 Combiner

The combiner compares the magnitudes of the I-channel and Q-channel output signals from the MTI filters and obtains a magnitude approximation by summing the greater of the two with half the lesser. This is a relatively easy way to obtain the approximate magnitude of two vectors ($I^2 + Q^2$) using simple hardware circuits. The results are non-coherently integrated and then passed on to other devices as required.

4.4.3 Integrator

The integrator is a non-coherent accumulator with a 512 range-cell capacity. For each range, the content of the memory cell for that range is read out, summed with the new data from the combiner and re-entered in the memory. On the last batch of pulses being processed (Mth pass), the data are fed to the CFAR detector and, if required, can be simultaneously entered in the integrator memory, or the memory can be cleared, ready for further processing. If the entries are made in the memory, the contents can be read by the computer. The process of reading the memory automatically clears it.

4.4.4 CFAR Detector

The CFAR detector forms part of the signal processor unit (SPU) which is used in the Adaptive Radar system in conjunction with the MTI filters, combiner and integrator. The MTI operates as a batch processor, the processed data from each batch being stored in the integrator. Accumulated data are fed to the CFAR detector, on a cell-by-cell basis, as returns from the last batch are being processed.

The CFAR detector uses range cell averaging to generate a reference threshold based on the resultant average to obtain a constant false alarm rate (P_{fa}), Figure 7. It adaptively selects between the reference threshold derived from averaging and that derived from a range-dependent

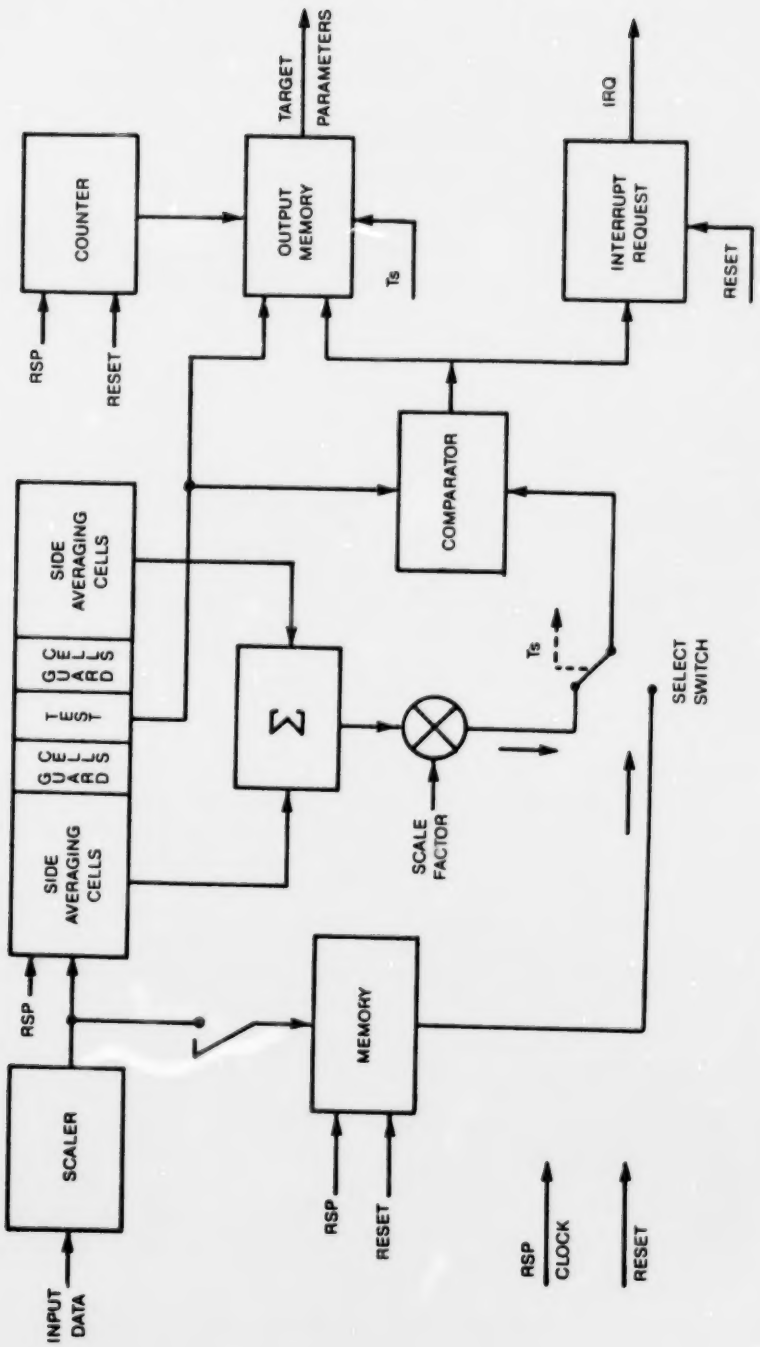


Figure 7 - CFAR Detector

average previously stored in an internal memory (sigma memory), and sets the threshold offset to fix the P_{fa}. If required, the operator can select between the range cell averager and sigma memory levels. A return signal in the test cell whose magnitude exceeds the threshold level is treated as a target detect. The detection parameters of targets are entered in a CFAR output memory and, on completion of the CFAR process, a computer interrupt is sent to the computer to allow the computer to take appropriate action.

The sigma memory levels are formed by measuring the mean value of the system thermal noise as a function of range (modified by the action of the sensitivity time control (STC) attenuator). This is achieved by executing dummy runs with the transmitter turned off and entering the averaged ouput noise magnitudes in the memory.

The averager threshold is derived through the use of a conventional range cell averager. Range cells on the near and far sides of a test cell are used to generate an estimate of the mean value of the return signals. The test cell is isolated from the averaging cells by guard cells which border the test cell. Both the number of averaging cells and the number of guard cells used in this process are programmable.

4.5 Range and Azimuth Gates

The system has provision for the insertion of single-window or triple-window data selection range gates and azimuth gates. These can be used to gate the data being selected or to control various devices. They provide a means of selectively gating the data flow to the devices and minimizing the possibility of overflow. The gates are individually controlled by the radar control program.

5. Control Computer-to-Display Computer Link

A two-way link connects the control and display computers. This link allows files or data messages to be transferred between the two. Several types of message can be transferred, each requiring a different response from the receiving computer. Disk files from either computer are generally transferred for storage on disk. Data transfers from the control computer are for display updates or possibly for processing, such as for plot extraction. Data transfers from the display computer to the control computer are the results of processing.

Transfers are initiated by sending a code number identifier on the link. This identifier is acknowledged by being echoed back. The message is then sent and upon completion of the transfer, is acknowledged by the receiving computer by adding 100B (B=OCTAL) to the message code number and sending it back to the sender. As transfers can be initiated from either end, a conflict could arise if both ends initiate a transfer at the same time. To prevent this, transfers from the control computer are given priority.

Code numbers in the range 1 to 77B are assigned to the control computer and 200B to 277B to the display computer. Numbers with the bits corresponding to 100B are not used as 100B is the acknowledgement flag which indicates that the transfer is complete.

6. Control Computer-to-VAX Link

The link between the control computer and the VAX allows files and data or commands to be transferred between the two computers and, in addition, allows data to be transferred from the radar data storage buffers and other radar sub-systems, such as the CFAR, on the Radar System Bus directly to the VAX computer. Communication between computers is two-way. Communication between devices on the Radar System Bus and the VAX is one-way. The control computer normally maintains full control of the Radar System. However, control can be transferred to the VAX allowing the experimenter to control the system from his own keyboard or from his experimental program.

A message identification system using code numbers is used to control the flow of data through the link. To prevent conflicts when both computers request the link simultaneously, priority is given to the VAX. A transfer is initiated by interrupting the receiving computer and transferring a two-word message over the link. The first word transferred is the message code number. The second word is the message word count. The receiving computer can then ready its input to receive the specified number of words (2-byte words). The code number determines the destination of the message.

6.1 Control of the Radar System Through the Link

The technique of passing coded message identifiers between the two systems allows a user to control the system from the VAX computer, either from a user's program directly or through the user's keyboard. The radar system is operated from a block of parameter tables stored in the radar control computer memory. These parameter tables can be transferred over the link to the VAX, modified as required by the user, and returned to the radar control computer. The parameters are used to run the radar when a "RUN" instruction is received.

The VAX instruction set is stored in a library and can be called by simple subroutine calls in the user's program. These are loaded into memory as part of the user's program. The radar can then be operated by calling the subroutines with appropriate parameters.

7. Control Software

The radar is centrally operated from a standard computer terminal and keyboard. The operator has control over all aspects of the radar including the system configuration, radar parameters, scanning modes, MTI filtering, CFAR detection and data handling.

The basic concept used in the design of the control program was to make the system as flexible as possible and yet simple to operate, as well as being configured so that it could be easily understood by various programmers. To simplify the operation, the program was designed with a large number of prompts that lead the operator through the program most directly or, if necessary, allow him to jump back and forth in the programs required to make new entries or any changes that might be required. To simplify programming, a subroutine was written for each recognizable or frequently used function. Where possible, these subroutines were given recognizable names that can be related directly to their particular function. The subroutines were grouped into segments on a functional basis and each segment given a name related to its function. Utility subroutines are generally placed in the main or executive part of the program.

The prompts used are very specific and request the operator to enter the various system parameters or instructions required. The entries are checked against limits or other system criteria and, if acceptable, are entered in system parameter tables for use by the system run routines. If an error is detected, an error message is displayed on the console CRT and the last prompt is repeated. If the operator needs assistance, entering a 'Q' or '?' will invoke the Menu and a list of acceptable responses will be displayed on the CRT.

The program consists of the memory resident main executive and several first and second level segments. The first level segments are called from the executive and in turn, call the second level segments. The segments are only called during the initial set-up stage. During the run stage, a run segment remains in memory and controls the operation of the system.

Figure 8 is an overview showing the signal paths between the executive and the main system segments. Those used for a normal operation consist of a 'Configuration', 'Multiplexer', 'Parameter Definition' and 'Run' segment. Data transfers between the segments or to the executive are through the common storage area, which is part of the executive and remains memory-resident.

Other segments include a 'Menu' segment which contains a list of instructions, a 'Test' segment, and a 'VAX' link control segment. Special segments can easily be added to the system as requirements arise. Calls to the menu are controlled by flags. These allow the menu to be called from any point in the program and to return to the calling point. The test segment contains a comprehensive list of tests that can be called from the run segment when the system is in a quiescent mode. Test returns to the run segment on completion of the test. The remaining segments are special segments required for specific operations such as data collection, etc.

Summary and Comments

The experimental radar system described in this report is a highly

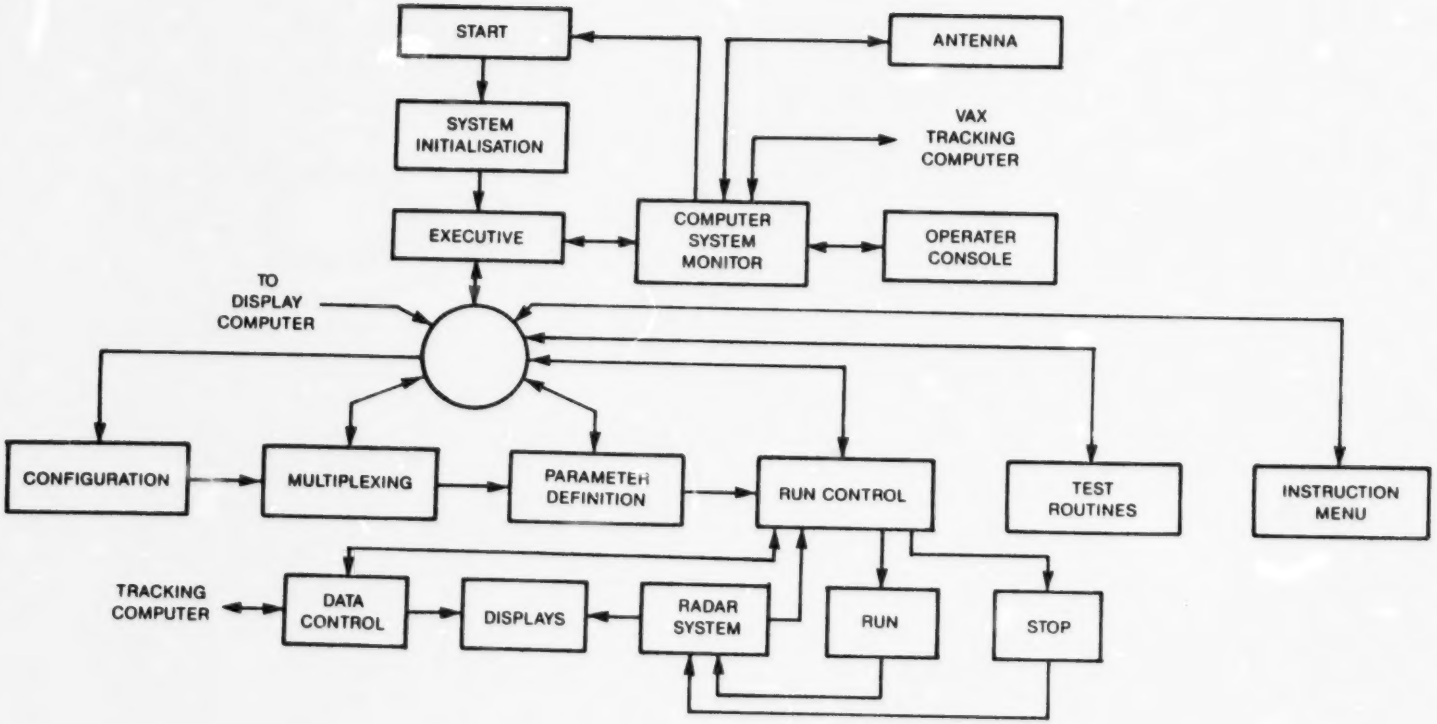


FIGURE 8: ADAPTIVE RADAR CONTROL PROGRAM

modularized phased-array radar system designed especially for use as a laboratory tool for experimenters. It can be used to study adaptive control techniques that can be applied to phased-array radar systems to take advantage of their flexible steering capabilities. A link between the radar system and a Digital Equipment VAX 11/780 computer allows experimenters to acquire real-time or non real-time radar data for analysis, and also to control the operation of the radar system from the VAX.

Development of the system is an on-going process and can be redirected as required to satisfy the changing requirements of experimenters.

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APPENDIX A

RADAR CHARACTERISTICS

1. Antenna

(a) Space fed plane array

No. of elements	295
Aperature (oval)	1.11m x 1.6m
Beamwidth	4° Az., 6° El.
Beam switching time	20 usec
Coverage*	80° Az., 30° El.
Sidelobes	-22 db
Height	62 feet above ground level

(b) Parabolic reflector mounted on El/Az positioner

Aperature	6'
Rotation	2 RPM max.
Beamwidth	3°
Height	72 feet above ground level

2. Transmitter

TWT power amplifier	L-5569 51
Frequency range	2.9-3.1 GHz
PRF*	153 Hz to 4166 Hz
Peak power	3.5 kW

3. Coherent Frequency Sources

Intermediate frequency	60 MHz
Local oscillator frequency**	2910 MHz
Synthesized frequency range*	2840 to 3040 MHz (usable range)

4. Receiver

System noise figure	7 db
RF bandwidth	30 MHz
RF gain	35 db
RF level control (attenuation)*	0 to 81 db
IF bandwidth (filters)**	1, 2 and 4 MHz
IF gain range**	25 to 85 db
IF level control (attenuation)	0 to 42 db
Linear and logrithmic IF amplifiers**	

* programmable feature

** device selectable feature

5. Detector

   Linear amplifier detector**
   Logarithmic amplifier detector**
   Linar amplifier synchronous detector

6. Waveform Generator & Synchronizer

Pulse width*	0.2 usec up (duty cycle limited)
Pulse burst*	duty cycle limited
PRF*	153 Hz to 11.9 KHz
PN code subpulse	External modulation
Range sample pulse (max. rate)	3.3 MHz

7. Signal Processing

I & Q channel ADC's	12 bits, 5 MHz max. rate
MTI filters (I & Q)*	2 to 16 pulse cancellation
CFAR detection*	range cell averaging
Links to external processors	
High speed buffers*	

8. Control System

   Hewlett Packard 21MX computer
   Digital sub-system control bus (in-house designed)
   Receiver sub-system control bus (IEEE 448)

9. Calibration and Test

   Modulated RF* (pulsed)
   CW RF*
   Doppler simulation*
   Phased array BITE test system*
   Sub-system BITE test system and software tests*

10. Displays

   PPI display*
   Graphics display
   Link to display computer

* programmable feature

** device selectable feature

APPENDIX B

TIMING DIAGRAMS

The primary timing clock in the radar is a 10-MHz clock derived from the 60-MHz IF reference source. This clock is enabled by a run instruction and turned off by a stop instruction. A secondary timing clock is a 15 MHz clock that is also derived from the 60-MHz reference source. The 15-MHz clock is used to generate range sample pulses and is gated on after each radar transmit pulse and off prior to the next one.

The basic radar timing pulse is the transmit pulse. The repetition interval of this pulse (PRI), Figure B1(a), is shown in the range 83 to 6500 microseconds. The lower limit is actually a function of the maximum allowable transmitter duty cycle and of the control software. As it currently exists, the minimum PRI is limited to 300 microseconds by the software.

Each transmit pulse is accompanied by a group of timing pulses required to synchronize and otherwise control the system, Figure B1(b). A list of these pulses is given below:

	Pulse	Function
1.	10-MHz clock	The main timing clock in the radar
2.	15-MHz clock	Clocks the range-sample pulses
3.	Pre-TX pulse	The pre-transmit pulse
4.	Beam Switching pulse	Synchronizes the antenna array to the radar
5.	TWT pulse	Modulates the TWT
6.	RF Modulation pulse	Produces the RF pulse
7.	Zero-Reference delay	Times the start of the range-sample pulses
8.	Range Sample pulses	Triggers the return signal sample circuits

The pulses are available throughout the system to synchronize various hardware modules.

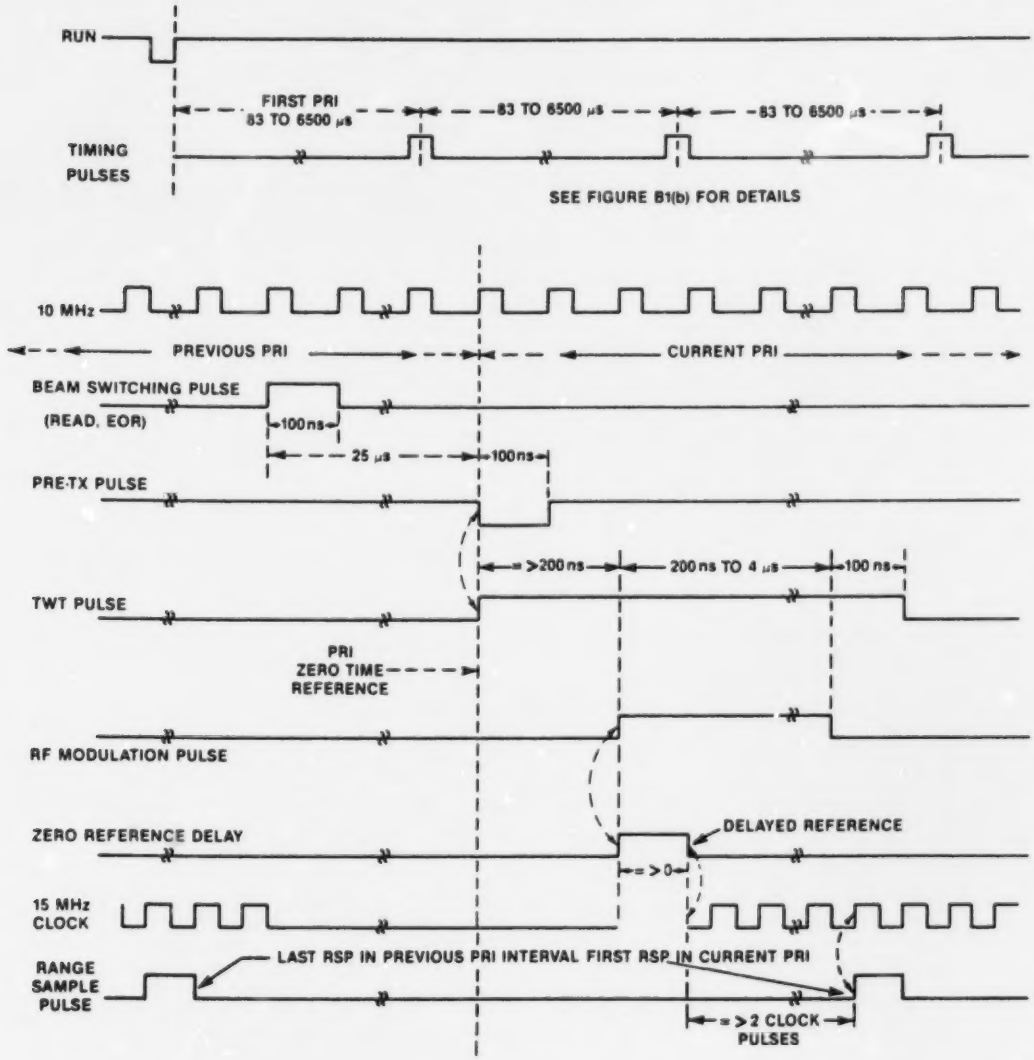

Figure B1 - Timing Diagram

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13. ABSTRACT

An experimental S-band phased-array radar system developed at the Communications Research Centre is described. The system was developed to provide experimenters with a means of acquiring real-time radar data for on-line or off-line analysis and to establish a test bed for new experimental devices or data processing techniques.

The system is built in modular form, thus allowing various parts of the system to be easily interchanged with experimental devices. It is linked to a Digital Equipment Corporation 11/780 VAX computer which allows data to be transfered from the radar to the VAX in real time, or to be stored in high-speed buffers and then transferred in blocks directly from the buffers to the VAX. The experimenter, using the VAX, can adaptively control the radar, request new beam directions, control data acquisition, etc., via the link.

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Adaptive

Radar

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